

FIG. 1

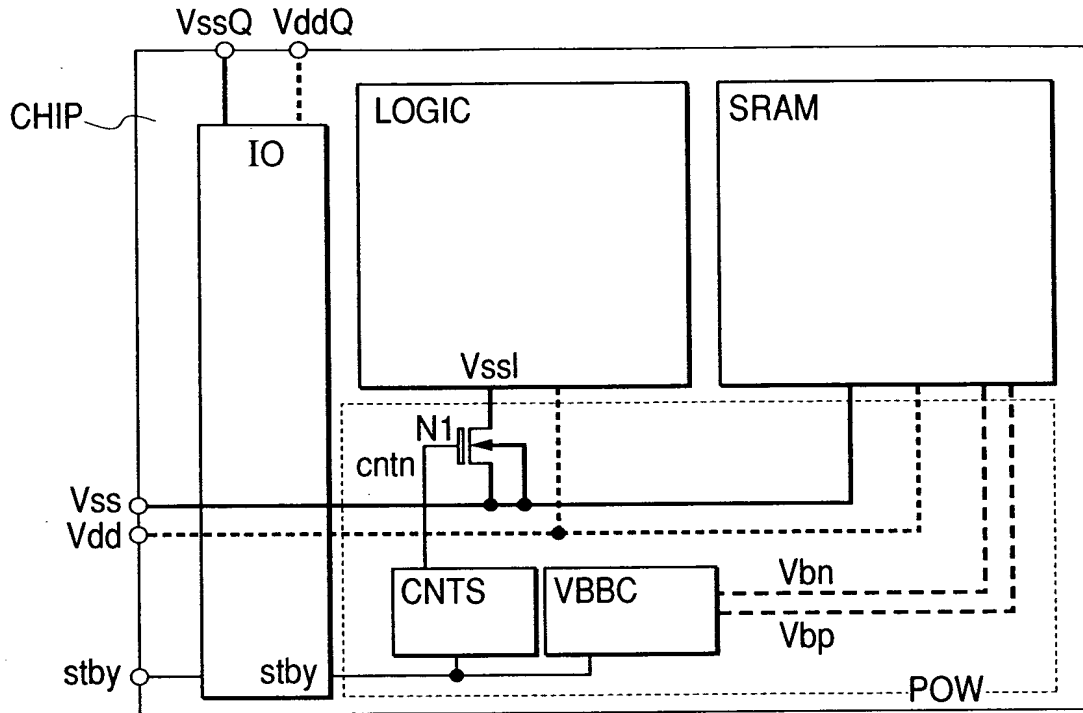


FIG. 2

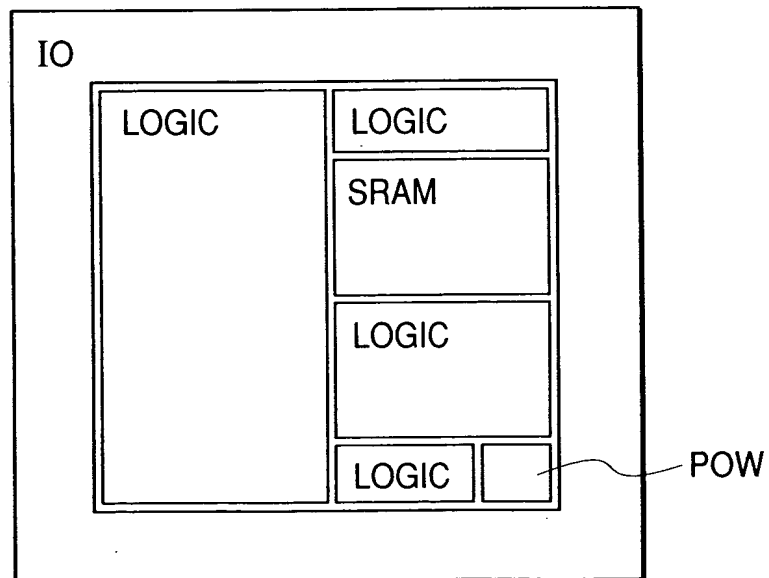


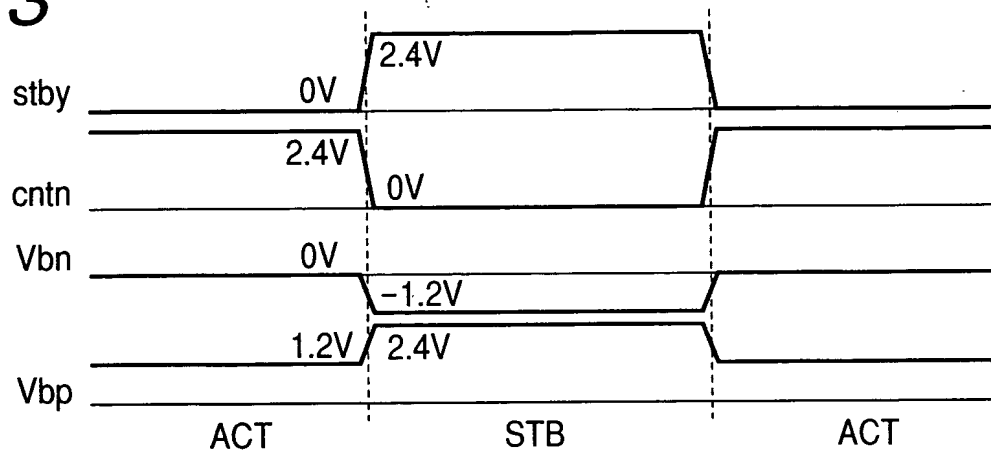
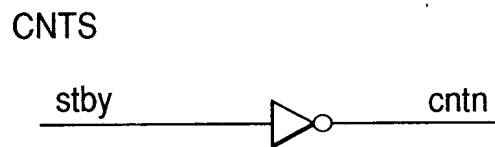
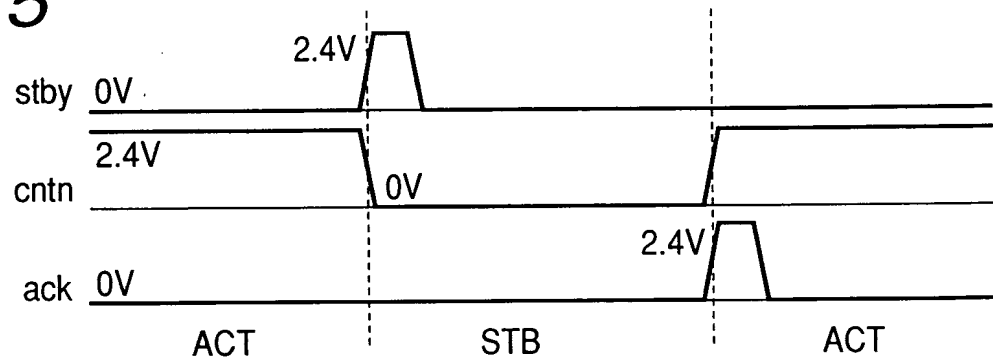
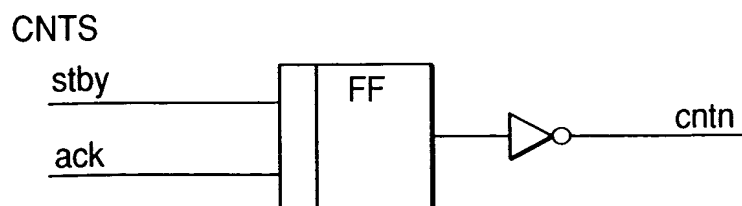
FIG. 3**FIG. 4****FIG. 5****FIG. 6**

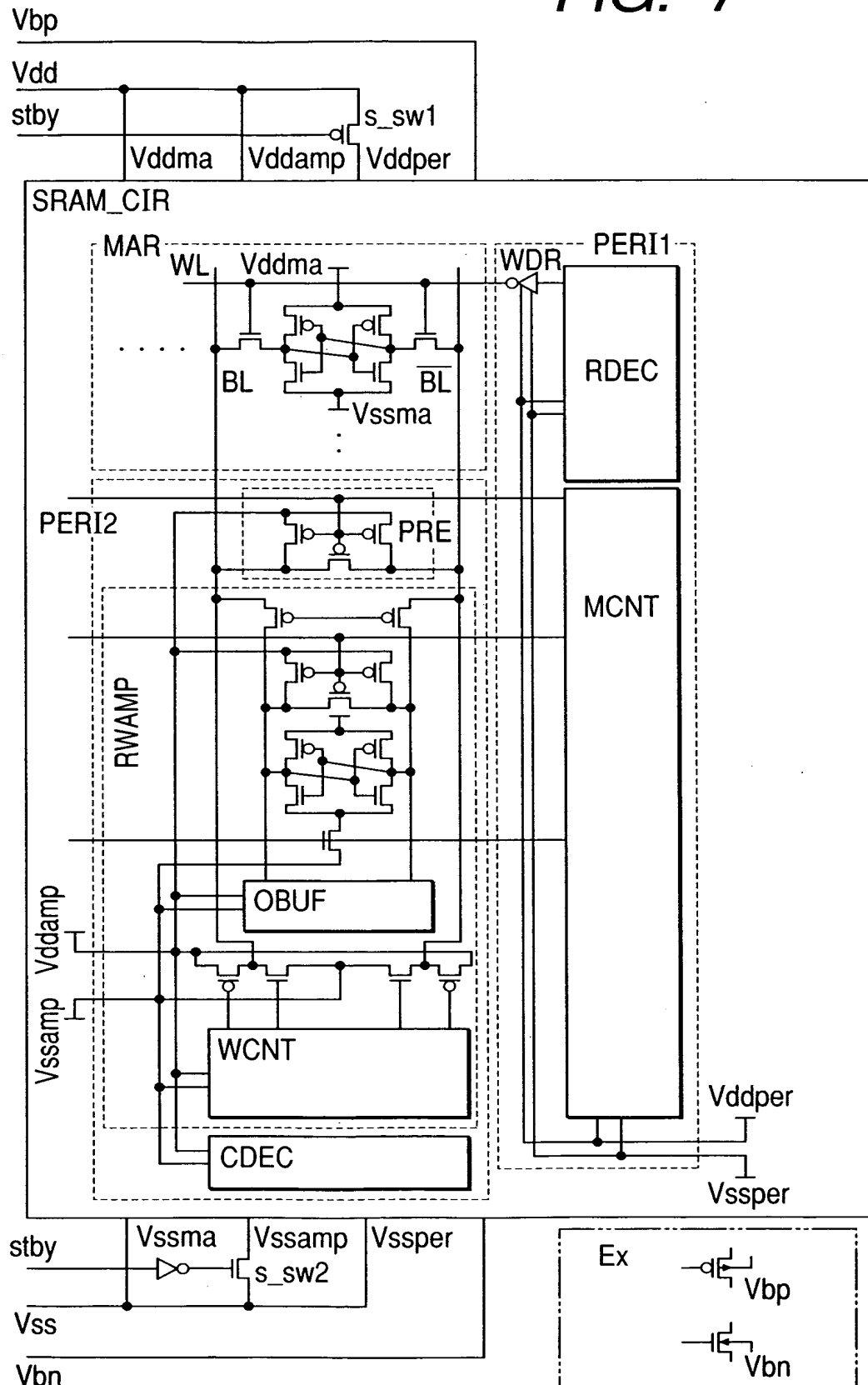
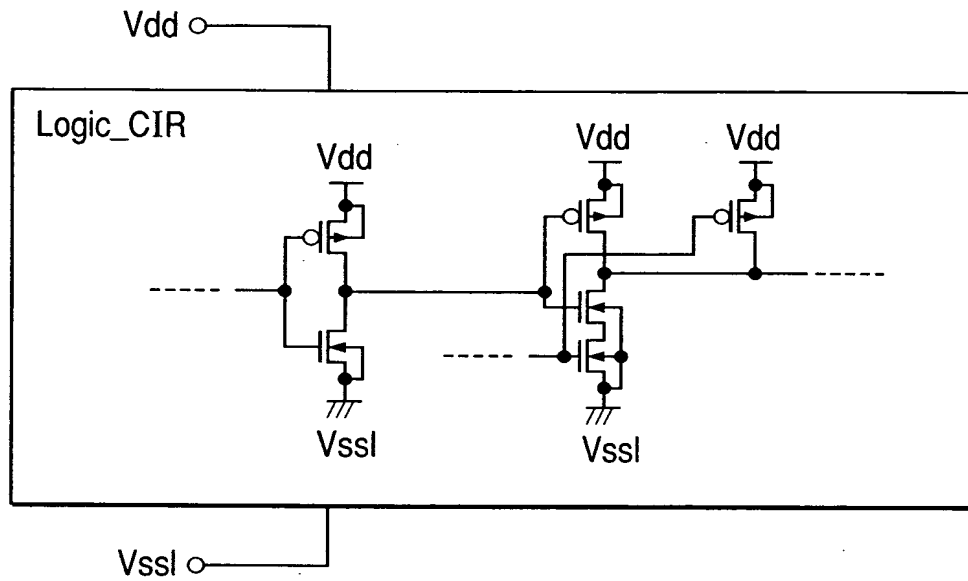
FIG. 7

FIG. 8**FIG. 9**

		Logic_CIR	Logic sw (N1)	SRAM_CIR	SRAM sw (s_sw1, s_sw2)	IO
Pattern1	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	2.0nm 0.40V	6.7nm 0.80V
Pattern2	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	6.7nm 0.40V	6.7nm 0.80V
Pattern3	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V, 0.40V	2.0nm 0.40V	6.7nm 0.80V

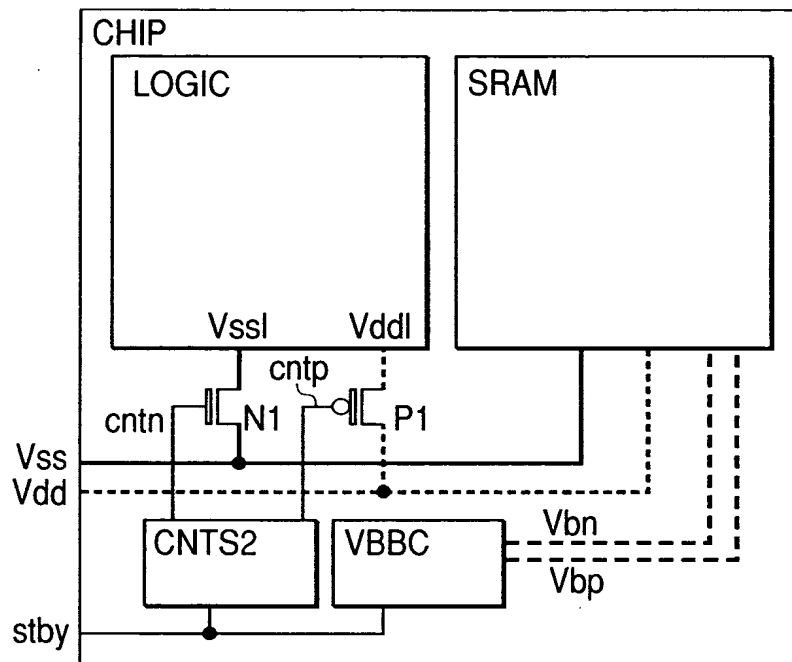
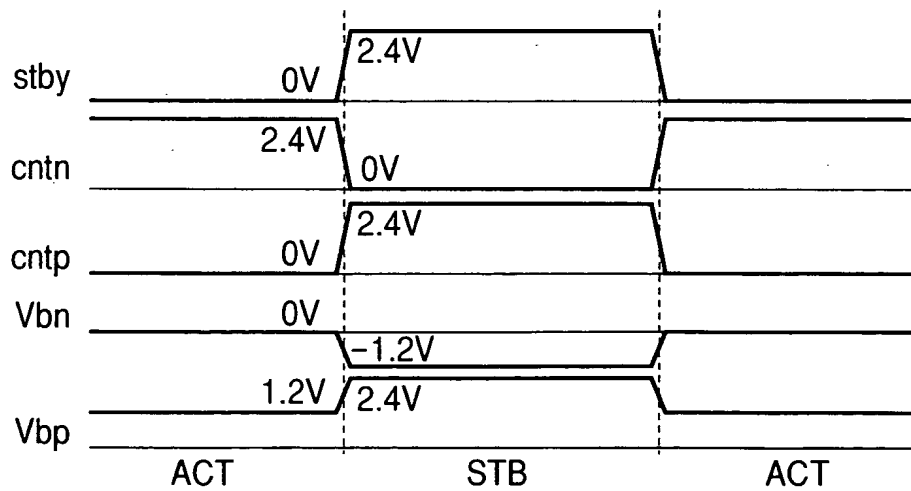
FIG. 10**FIG. 11**

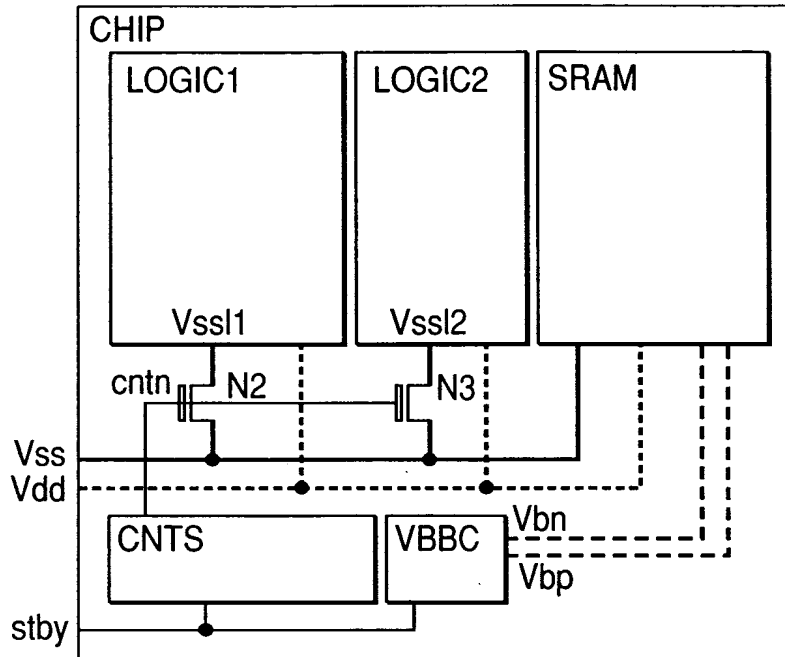
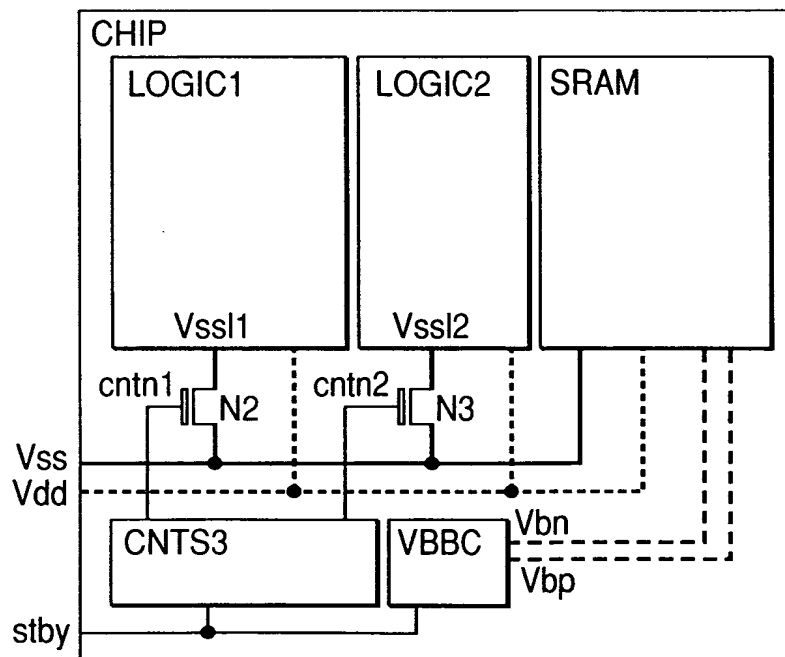
FIG. 12*FIG. 13*

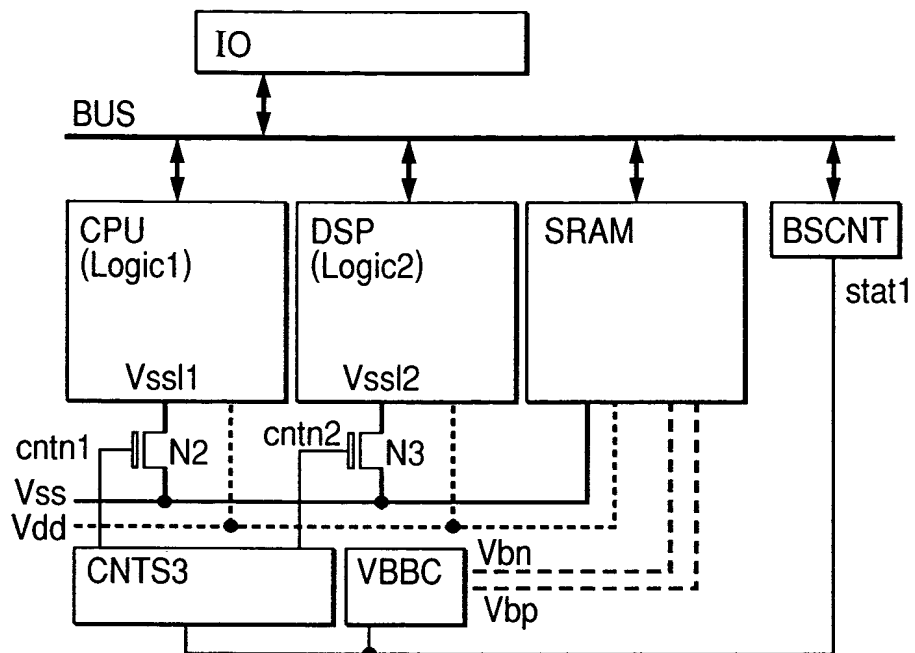
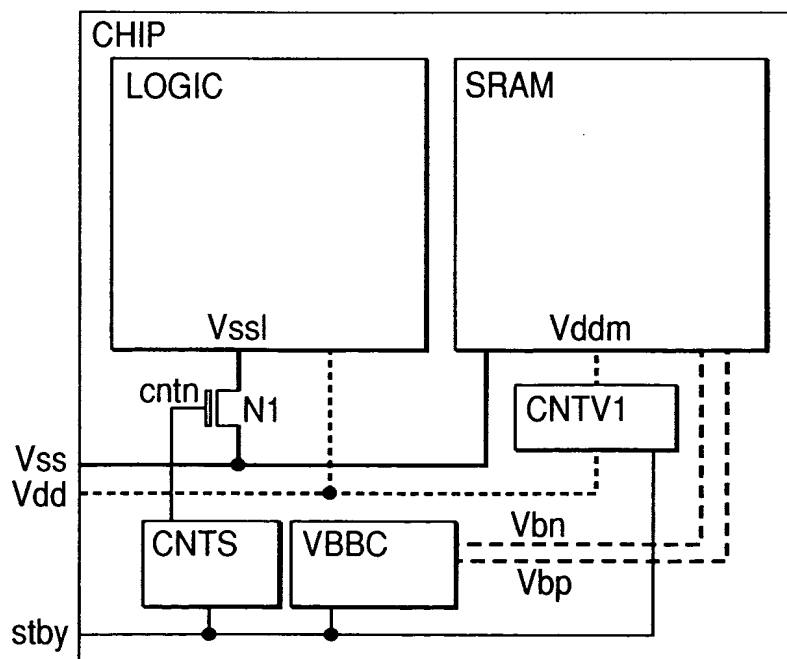
FIG. 14*FIG. 15*

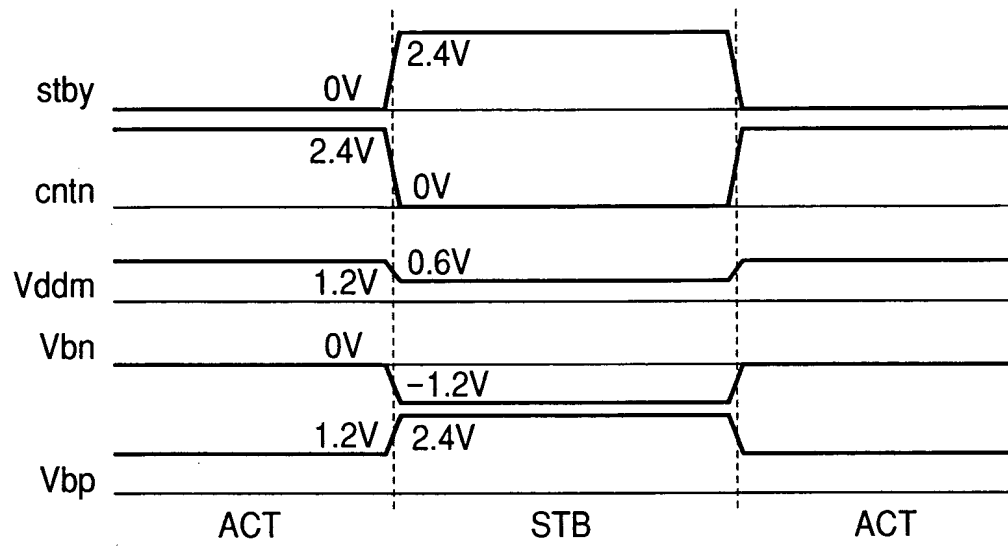
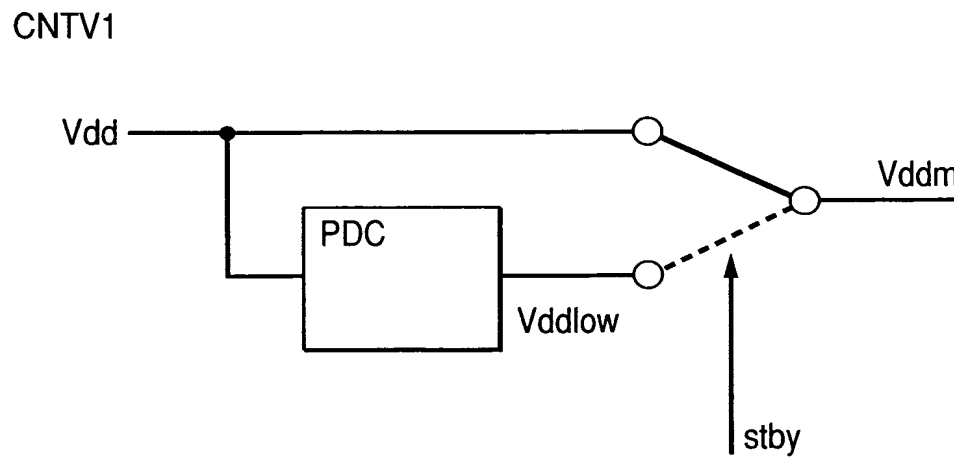
FIG. 16*FIG. 17*

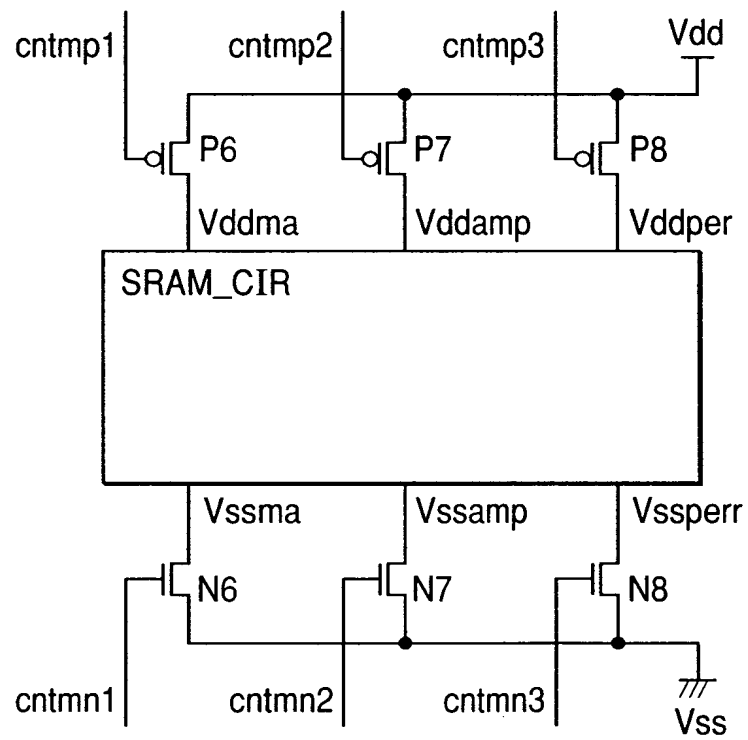
FIG. 18

FIG. 19

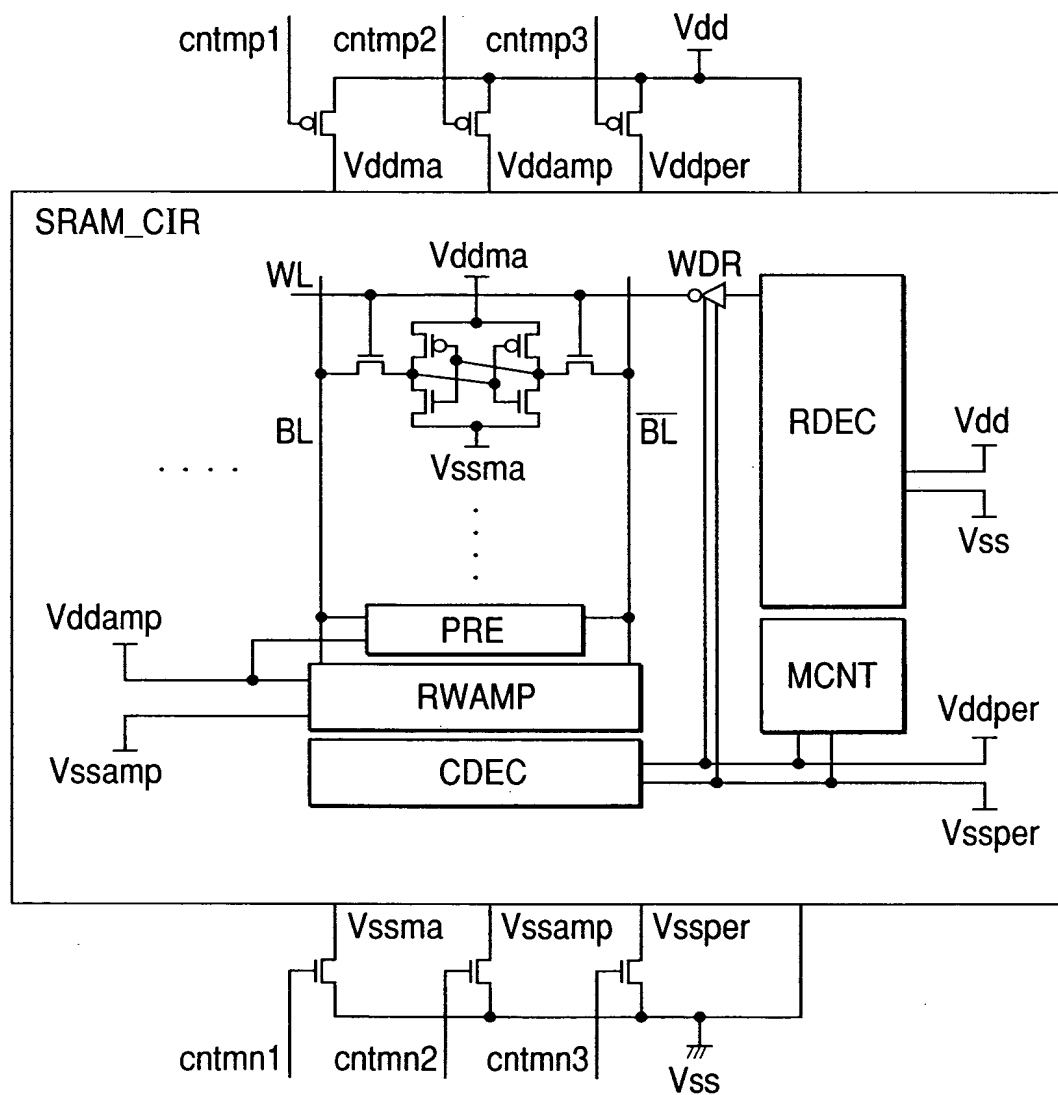


FIG. 20

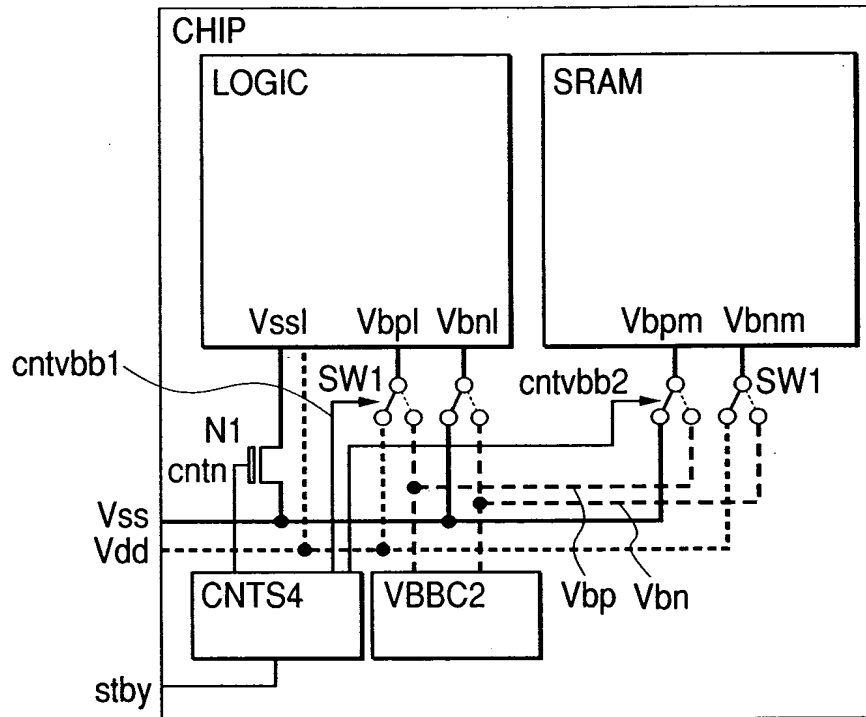


FIG. 21

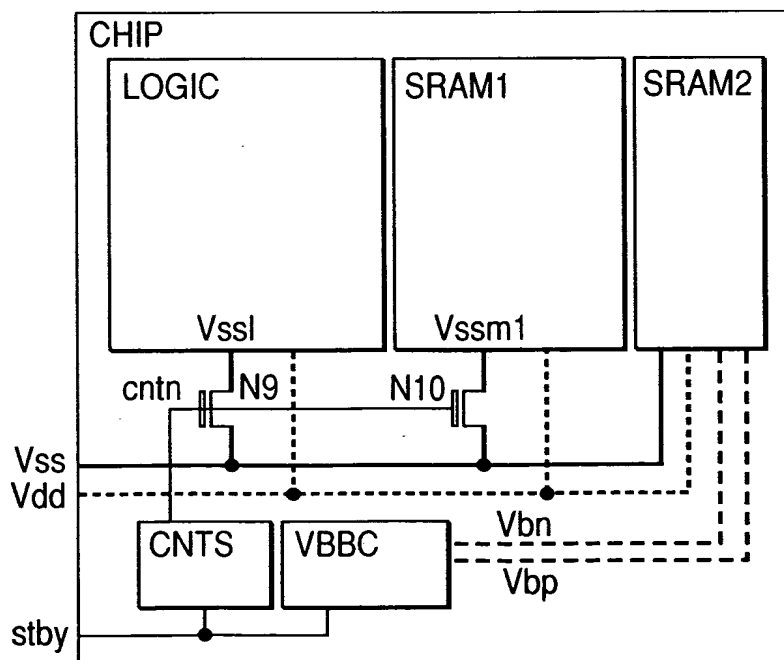
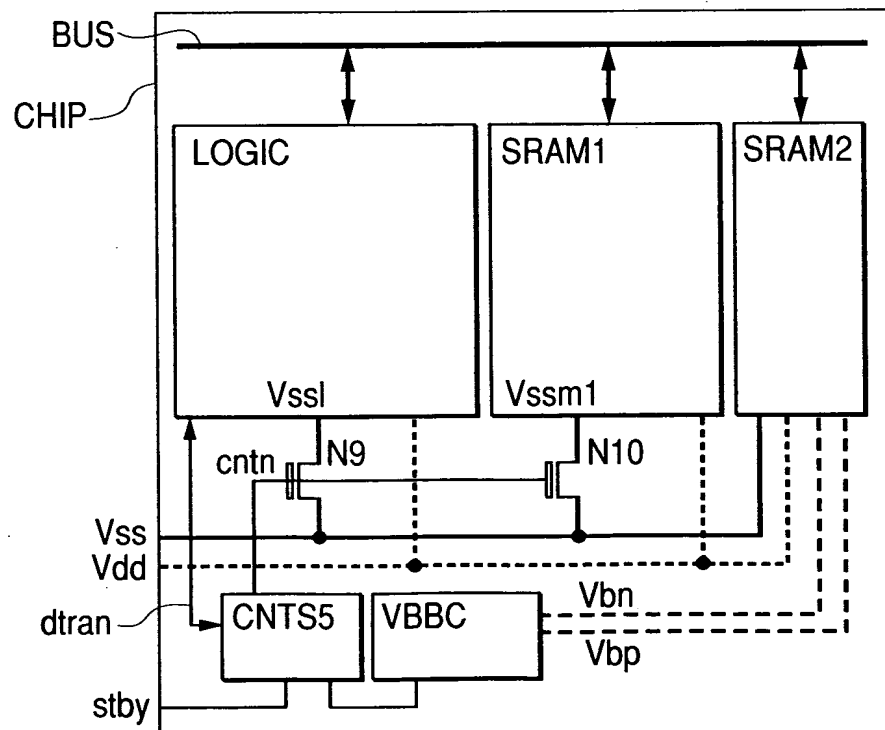


FIG. 22

		Logic_CIR	IO	MAR1	MAR2
Pattern1	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.40V	2.0nm 0.40V
Pattern2	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.40V	6.7nm 0.40V
Pattern3	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V	2.0nm 0.40V
Pattern4	Tox Vth	2.0nm 0.25V, 0.40V	6.7nm 0.80V	2.0nm 0.25V	6.7nm 0.40V

FIG. 23

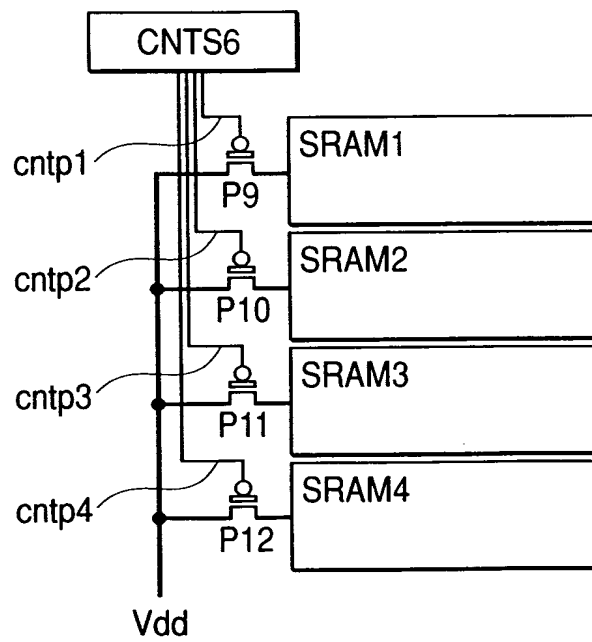
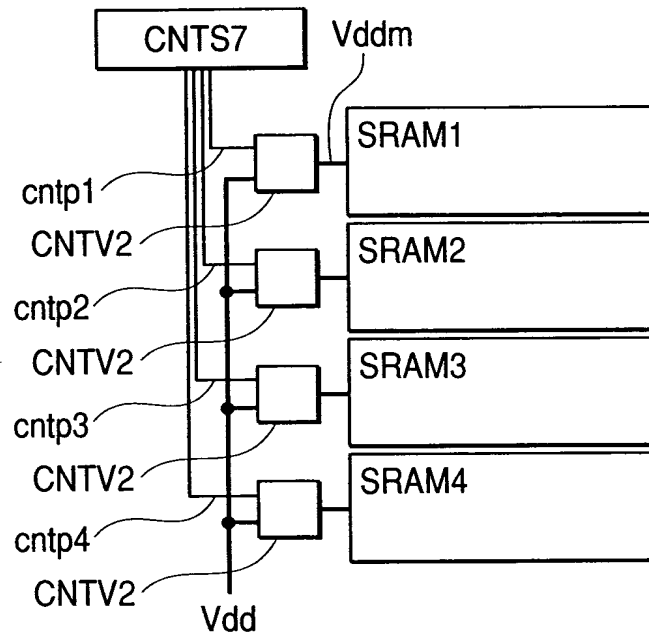


FIG. 26